Word Error Rate Measurement Methodology and Characterization Results

The Word Error Rate (WER) specification of Analog to Digital Converters (A/D) is of particular interest to certain applications. Typically, these applications are sensitive to events during which the A/D digital sample produced deviates significantly from the analog input voltage, even if such an event is exceedingly rare. This application note reviews Intersil's WER measurement methodology and characterization results for the KAD5xxx family of converters.

- WER measurement methodology and test setup reviewed
- Detailed characterization results reviewed
  - Measured WER = 8.9E-13
  - Measured WER with "worst-case" analog input was similar
- Largest WER code weight measured was 37 codes. This is due to Intersil's unique architecture, which limits the code weight of WER events

Measuring an extremely low probability event such as WER can be difficult. As an example, assume a 100MSPS, 12-bit A/D with a WER specification of 1E-12. Requiring a 100 times oversampling of the error condition would necessitate capturing 1E14 ADC samples. This data capture would require over 11 days of continuous sampling to gather, and would consume over 150TB to store the data, not to mention the details of how to process the data. Clearly this brute force approach is unwieldy at best. An alternative methodology and results are described in the following.

The test setup used for measurement of WER at Intersil is illustrated in Figure 1.

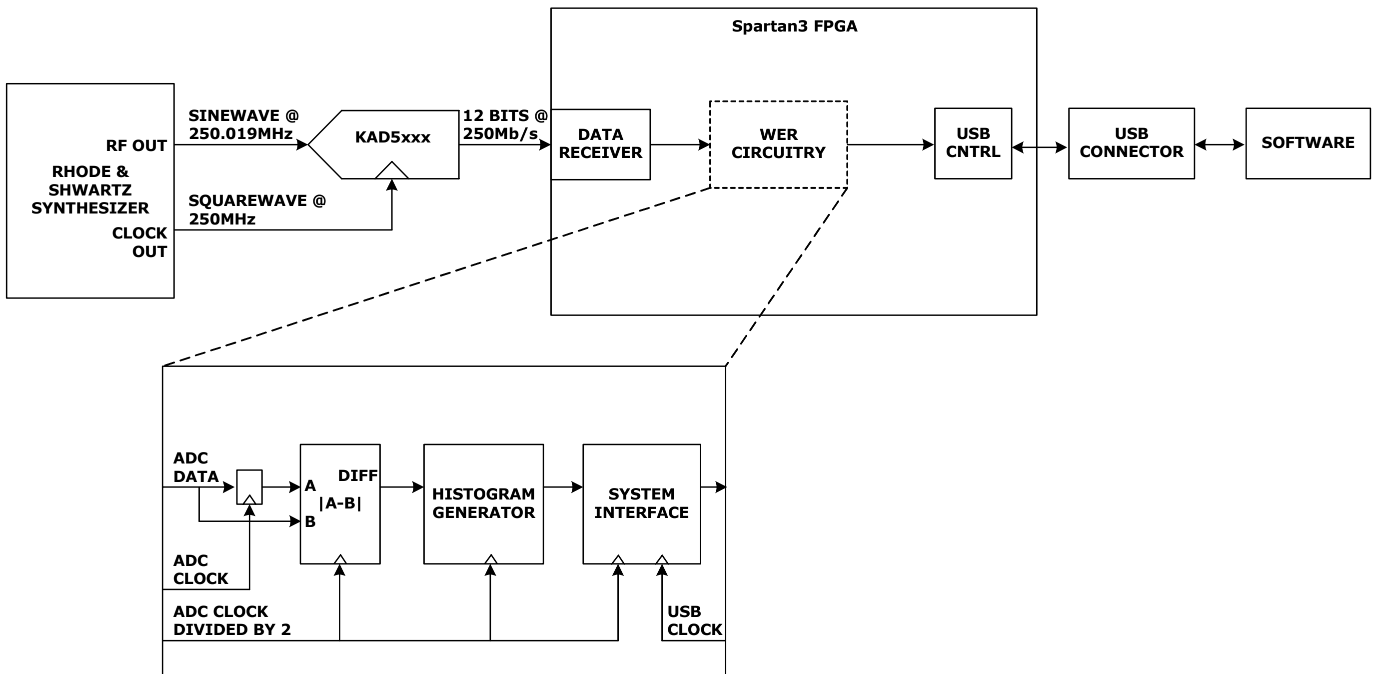

FIGURE 1. WER TEST SETUP

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This test concept is based on known techniques [1] for accurately measuring WER in an analog to digital converter (A/D). Using an input sinusoid to the A/D that is slightly offset in frequency from an integer multiple of the sample rate creates output samples that slowly change value, while still exercising the converter at full sample rate and high input frequency. The samples from the A/D are then split into temporal pairs, and a difference is generated from each pair. Given the sparseness with which word error rates occur, the probability of generating two sequential samples with word errors is vanishingly small. Each difference is then recorded by a histogram generator. In the setup, the histogram generator consists of sixteen 47-bit up counters, where each counter is one of the histogram generator's bins. One counter is incremented on every difference taken. The histogram generator's bin values in digital codes are 0, 1, 2, 3, 4-7, 8-11, 12-15, 16-23, 24-31, 32-39, 40-47, 48-55, 56-63, 64-71, 72-79, and 80-4095. The amplitude of the input sinusoid for this measurement was 90% of full scale.

The resulting histogram is accumulated for some amount of time, as controlled by software. Note that each difference in the histogram represents testing of two unique samples. This algorithm ran continuously for several days, generating composite histogram data that represents word error rate measurements for approximately 8.2E13 samples. This number of samples is over eight times the minimum number of samples recommended by the IEEE standard [2] for a WER of 1E-12. The resulting composite histogram can be viewed in Figure 2.

Calculating the expected variation in difference values due to the sum of known processes is necessary to bound what constitutes word errors in the data. The formula in Equation 1 illustrates the terms used to calculate this bound, with a brief description of each term following:

$$Bound \cong SD_{thermal_noise} + SD_{Slope} + SD_{DNL} + SD_{RMS_jitter} \quad \text{(EQ. 1)}$$

$$Bound \cong \frac{3}{4} * 8 * \sqrt{2} + 1.42 + 2.0 + 2.3 = 14.2 codes \quad \text{(EQ. 2)}$$

The standard deviation of thermal noise (kT/c) in each sample is approximately ¾ of a code (based on the SNR of the ADC). A multiple of this standard deviation must be found such that there is high confidence we will not observe this level of variation from the mean in the number of samples in the dataset (eight standard deviations was chosen). The difference of two uncorrelated, normal distribution samples will have a standard deviation of the root-mean-squared of the standard deviation of the two inputs. An additional term in the word error bound is caused by the expected maximum slope of the input sinusoid (1.42 codes per clock period), which directly adds 1.42 codes to the bound. Differential non-linearity adds approximately two codes to the bound, allowing an input voltage step of one nominal digital code between sample clocks to exhibit an actual code difference several times larger. Finally, the uncorrelated jitter between the clock and signal source adds some amount to the bound [1]. An estimate of the RMS jitter due to the KAD5xxx's clock receiver, aperture jitter, and uncorrelated noise between the synthesizer's clock and RF out is 70fs. Seven standard deviations yields, on average, approximately 210 events in a capture window the size of the number of samples taken. Once scaled for the maximum slew rate of the input sinusoid, and converted from volts per second to codes per second, we find that another 2.3 codes must be added to the bound to account for this effect.

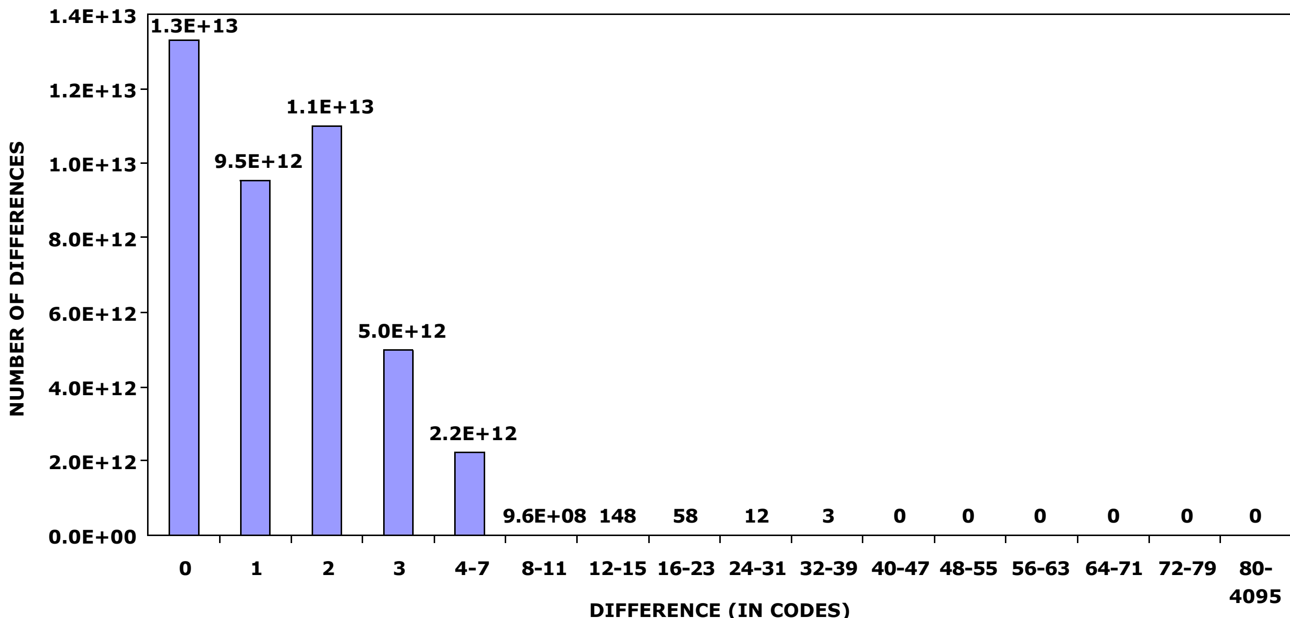

FIGURE 2. WORD ERROR RATE HISTOGRAM

Given the bound calculation in Equation 2, we would consider any differences larger than 14.2 codes to be word errors. The dataset indicates that there are 73 differences larger than 14.2 codes out of 8.2E13 samples, yielding an overall word error rate of 8.9E-13. Note the largest code difference that occurred in the entire capture was 37 codes.

The absence of large code weight errors in the resulting data showcases one of the architectural features of the KAD5xxx family of converters. One of the typical dominant sources of word errors in traditional converters is metastability in comparators. Such a WER event occurs when the input voltage to the pipeline stage is extremely close to the voltage threshold with which the comparator compares it, resulting in a classic metastability condition which can take an extraordinarily long time to settle. This event in a comparator can delay its decision about the input signal beyond the time allotted by the circuit design, which causes the analog domain adjustment to be out of sync with the information conveyed to the digital error correction (DEC) circuitry for that pipeline stage. The resulting word error code weight is directly related to the code weight of the pipeline stage at which the WER event occurred.

In contrast, for large code weight pipeline stages, Intersil's KAD5xxx converter uses a level-sensitive just in time analog domain adjustment. This just in time process allows the analog adjustment circuitry to act on delayed comparator decisions, correcting some significant portion of the word error in the analog domain. The end result of this process is that for metastability-induced delays in comparator decisions, the probability of a word error decreases exponentially with the code size of the error.

This is conceptually illustrated by probability distributions in Figure 3. The upper plot shows a traditional A/D, with metastability-induced word error probability distributions clustered around each pipeline stage's code weight. The lower plot shows Intersil's KAD5xxx converter metastability-induced word error probability distribution, which in effect creates a small code weight "tail" on the non-word error difference distribution.

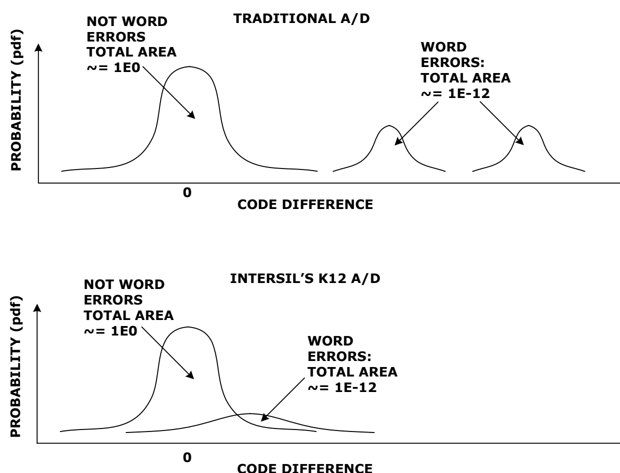

FIGURE 3. PROBABILITY DISTRIBUTIONS

Measurements were also taken to quantify the "worst-case" WER one could expect from the KAD5xxx converters in the presence of an engineered input. The measurement system was similar to the one described previously, with the modifications that the input sinusoid amplitude was set to 1% of full scale and a DC offset was added to the input signal. The added DC offset was adjusted such that it forced a 50% toggle rate of a particular comparator in the highest bit weight pipeline stage. This input signal has the potential to cause larger WER counts than a full scale sinusoid, because every sample has an input voltage very close to this particular comparator's threshold voltage. Data representing WER measurements for a total of 7.7E13 samples was gathered. The resulting composite histogram can be viewed in Figure 4 on page 4

As can be seen from the histogram in Figure 4, there is no significant increase in WER events with this engineered input signal. This measurement demonstrates from a practical point of view that the WER for the KAD5xxx converters is well bounded by the WER specification, even for specific waveforms that cause the input signal to be statistically likely to fall within the metastability window for a particular comparator.

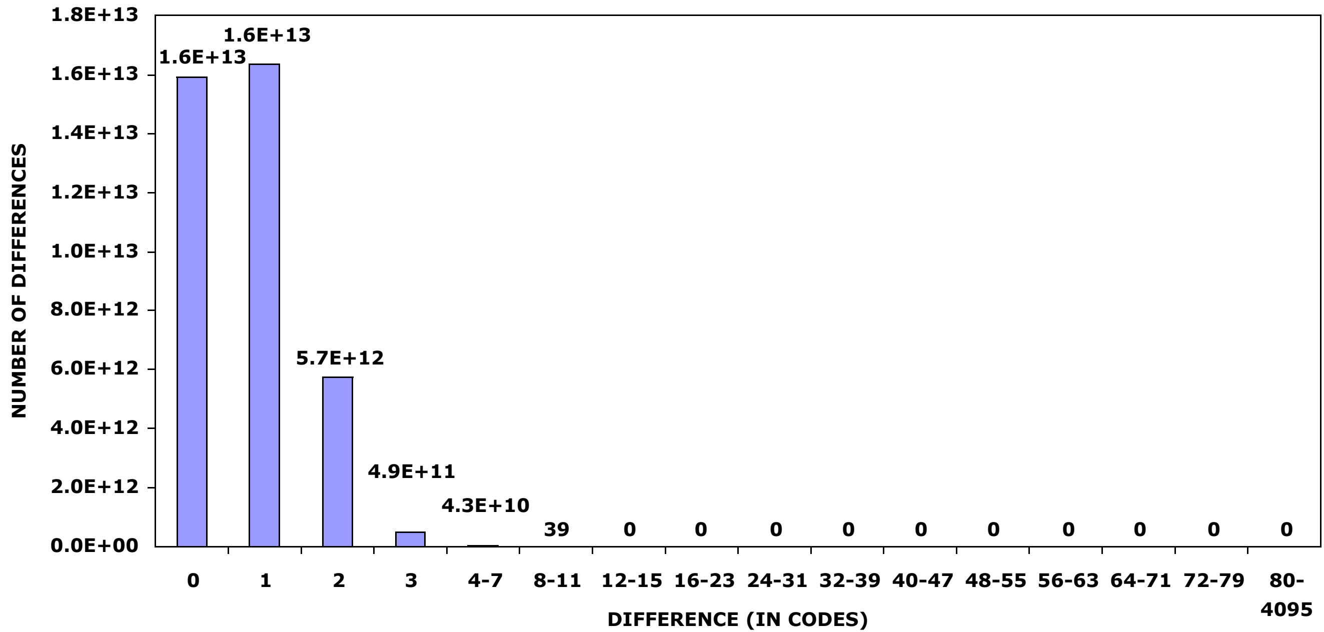

FIGURE 4. WORD ERROR RATE HISTOGRAM

References

[1] Chiorboli, G., De Salvo, B., Franco, G., and Morandi, C., "Some thoughts on the word error rate measurement of A/D converters", *IEEE International Conference on Electronics, Circuits and Systems*, Vol. 3, pp. 453 – 456, 1998

[2] IEEE Std. 1057-94, *IEEE Standard for Digitizing Waveform Recorders*, The Institute of Electrical and Electronics Engineers Inc., New York, December 1994.

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